ELCR-1040 Digital and Microprocessor Fundamentals
COURSE SYLLABUS
Spring Semester 2019

COURSE INFORMATION

Credit Hours/Minutes: 5 Hours / 5250 Minutes
Class Location: Gillis Building, Room 827, Vidalia Campus
Class Meets: Monday and Wednesdays (MW), 5:00 PM to 7:55 PM
Course Reference Number (CRN): 40097

INSTRUCTOR CONTACT INFORMATION

Instructor Name: William Greene
Office Location: Gillis Building, Room 822, Vidalia Campus
Office Hours: Monday through Thursday, 11:00 AM to Noon; Tuesday and Thursday, 1:00 PM to 3:00 PM
Email Address: William Greene (wgreene@southeasterntech.edu)
Phone: (912) 538-3102
Fax Number: (912) 538-3106

SOUTHEASTERN TECHNICAL COLLEGE'S (STC) CATALOG AND HANDBOOK

Students are responsible for all policies and procedures and all other information included in Southeastern Technical College's Catalog and Handbook (http://www.southeasterntech.edu/student-affairs/catalog-handbook.php).

REQUIRED TEXT

Digital Fundamentals, 11th ed.
by Thomas L. Floyd,
published by Prentice Hall,
ISBN# 0-13-273796-5

REQUIRED SUPPLIES & SOFTWARE

Engineering / Scientific Calculator (TI-83 Plus or better recommended)

Note: Although students can use their smart phones and tablets to access their online course(s), exams, discussions, assignments, and other graded activities should be performed on a personal computer. Neither Blackboard nor Georgia Virtual Technical Connection (GVTC) provide technical support for issues relating to the use of a smart phone or tablet so students are advised to not rely on these devices to take an online course.

COURSE DESCRIPTION

This course is designed to provide sufficient coverage of digital electronics and microprocessor fundamentals. Digital fundamentals will introduce basic topics such as binary topics such as binary arithmetic, logic gates and truth tables, Boolean algebra and minimization techniques, logic families, and digital test equipment. Upon

completion of the foundational digital requirements, a more advanced study of digital devices and circuits will include such topics as flip-flops, counters, multiplexers and de-multiplexers, encoding and decoding, displays, and analog to digital and digital to analog conversions. Students will also explore the basic architecture and hardware concepts of the microprocessor.

MAJOR COURSE COMPETENCIES / COURSE OUTLINE

1. Binary Arithmetic
2. Logic Gates & Truth Tables
3. Boolean Algebra & Minimization Techniques
4. Logic Families
5. Digital Test Equipment
6. Flip-Flops
7. Counters
8. Multiplexers & De-multiplexers
9. Encoding & Decoding
10. Displays
11. Analog-to-Digital and Digital-to-Analog Conversions
12. Microprocessor Based Systems and Architecture

PREREQUISITE(S)

ELCR 1020

GENERAL EDUCATION CORE COMPETENCIES

Southeastern Technical College has identified the following general education core competencies that graduates will attain:

1. The ability to utilize standard written English.
2. The ability to solve practical mathematical problems.
3. The ability to read, analyze, and interpret information.

STUDENT REQUIREMENTS

Students are expected to complete all tests and comprehensive problems by the due dates. A ten point penalty will be assessed for each day a comprehensive problem is late. There are no makeup tests. Tests are made available for several days; therefore, there are no makeup tests. Students who miss a test will be assigned a grade of zero. Students are responsible for policies and procedures included in the STC Catalog and Handbook. All online students must pledge that they have read and understand the STC Online Orientation within the first five days of class. Online students are responsible for checking e-mails and Blackboard announcements DAILY.

TRADITIONAL ATTENDANCE GUIDELINES

Class attendance is a very important aspect of a student's success. Being absent from class prevents students from receiving the full benefit of a course and also interrupts the learning process. Southeastern Technical College considers both tardiness and leaving early as types of absenteeism. Responsibility for class attendance rests with the student. Regular and punctual attendance at all scheduled classes is required for student success. Students will be expected to complete all work required by the instructor as described in the individual course syllabus.

Instructors have the right to give unannounced quizzes/assignments. Students who miss an unannounced quiz or assignment will receive a grade of 0. Students who stop attending class, but do not formally withdraw, may receive a grade of F and face financial aid repercussions in upcoming semesters.

Instructors are responsible for determining whether missed work may be made up and the content and dates

for makeup work is at the discretion of the instructor.

Students will not be withdrawn by an instructor for attendance; however, all instructors will keep records of graded assignments and student participation in course activities. The completion dates of these activities will be used to determine a student's last date of attendance in the event a student withdraws, stops attending, or receives an F in a course.

STUDENTS WITH DISABILITIES

Students with disabilities who believe that they may need accommodations in this class based on the impact of a disability are encouraged to contact the appropriate campus coordinator to request services.
Swainsboro Campus: Macy Gay mgay@southeasterntech.edu, 478-289-2274, Building 1, Room 1208
Vidalia Campus: Helen Thomas hthomas@southeasterntech.edu, 912-538-3126, Building A, Room 108

SPECIFIC ABSENCES

Provisions for Instructional Time missed because of documented absences due to jury duty, military duty, court duty, or required job training will be made at the discretion of the instructor.

PREGNANCY

Southeastern Technical College does not discriminate on the basis of pregnancy. However, we can offer accommodations to students who are pregnant that need special consideration to successfully complete the course. If you think you will need accommodations due to pregnancy, please make arrangements with the appropriate campus coordinator.
Swainsboro Campus: Macy Gay mgay@southeasterntech.edu, 478-289-2274, Building 1, Room 1208
Vidalia Campus: Helen Thomas hthomas@southeasterntech.edu, 912-538-3126, Building A, Room 108

It is strongly encouraged that requests for consideration be made **PRIOR** to delivery and early enough in the pregnancy to ensure that all the required documentation is secured before the absence occurs. Requests made after delivery **MAY NOT** be accommodated. The coordinator will contact your instructor to discuss accommodations when all required documentation has been received. The instructor will then discuss a plan with you to make up missed assignments.

WITHDRAWAL PROCEDURE

Students wishing to officially withdraw from a course(s) or all courses after the drop/add period and prior to the 65% point of the term in which student is enrolled (date will be posted on the school calendar) must speak with a Career Counselor in Student Affairs and complete a Student Withdrawal Form. A grade of "W" is assigned for the course(s) when the student completes the withdrawal form.

Important – Student-initiated withdrawals are not allowed after the 65% point. After the 65% point of the term in which student is enrolled, the student has earned the right to a letter grade and will receive a grade for the course. Please note: Abandoning a course(s) instead of following official withdrawal procedures may result in a grade of 'F' being assigned.

Informing your instructor that you will not return to his/her course, does not satisfy the approved withdrawal procedure outlined above.

There is no refund for partial reduction of hours. Withdrawals may affect students' eligibility for financial aid for the current semester and in the future, so a student must also speak with a representative of the Financial Aid Office to determine any financial penalties that may be accessed due to the withdrawal. A grade of 'W' will count in attempted hour calculations for the purpose of Financial Aid.

EXIT EXAM

This course, ELCR-1040, is the CAPSTONE course for the Electronics Technology Degree and Diploma Programs. Students are required to score a grade of 70% or higher on the Final Exam for this course. Students who score less than 70% on this exam will be awarded a grade of 0% for this exam and a failing grade for the class, requiring the student to retake this course to complete their respective program.

WORK ETHICS

The Technical College System of Georgia instructs and evaluates students on work ethics in all programs of study. Ten work ethics traits have been identified and defined as essential for student success: appearance, attendance, attitude, character, communication, cooperation, organizational skills, productivity, respect, and teamwork. Students will be required to take a work ethics exam as marked in the lesson plan. A grade of 70 or better is required to complete the work ethics requirements for this class.

MAKEUP GUIDELINES (TESTS, QUIZZES, HOMEWORK, PROJECTS, ETC.)

Students are required to take all tests and complete all assignments scheduled during the semester. Failure to take Tests/Exam(s) and complete assignments will result in a grade of zero. There will be no makeup of assignments or EXAMS. If Internet or browser failure occurs, contact instructor immediately. A decision will be made at that time if the exam will be reset. Instructor reserves the right to deduct points from the exam scores for exceeding the scheduled time limit on the exam and/or requiring student to come to campus to take the final exam. Note: If student notifies instructor about exam problems because of technical issues after the due date or on the last day of the semester, the student will NOT be allowed to make-up the exam. No exceptions! Assignments must be turned in on the assigned date and will not be accepted late, a grade of zero will be given. ALL Assignments are due according to the lesson plan.

ACADEMIC DISHONESTY POLICY

The Southeastern Technical College Academic Dishonesty Policy states that all forms of academic dishonesty, including but not limited to cheating on tests, plagiarism, collusion, and falsification of information, will call for discipline. The policy can also be found in the Southeastern Technical College Catalog and Handbook.

PROCEDURE FOR ACADEMIC MISCONDUCT

The procedure for dealing with academic misconduct and dishonesty is as follows:

1. **First Offense**
   Student will be assigned a grade of "0" for the test or assignment. Instructor keeps a record in course/program files and notes as first offense. The instructor will notify the student's program advisor, academic dean, and the Registrar at the student's home campus. The Registrar will input the incident into Banner for tracking purposes.
2. **Second Offense**
   Student is given a grade of "WF" (Withdrawn Failing) for the course in which offense occurs. The instructor will notify the student's program advisor, academic dean, and the Registrar at the student's home campus indicating a "WF" has been issued as a result of second offense. The Registrar will input the incident into Banner for tracking purposes.
3. **Third Offense**
   Student is given a grade of "WF" for the course in which the offense occurs. The instructor will notify the student's program advisor, academic dean, and the Registrar at the student's home campus indicating a "WF" has been issued as a result of third offense. The Vice President for Student Affairs, or designee, will notify the student of suspension from college for a specified period of time. The Registrar will input the incident into Banner for tracking purposes.

STATEMENT OF NON-DISCRIMINATION

The Technical College System of Georgia and its constituent Technical Colleges do not discriminate on the basis of race, color, creed, national or ethnic origin, sex, religion, disability, age, political affiliation or belief, genetic information, disabled veteran, veteran of the Vietnam Era, spouse of military member or citizenship status (except in those special circumstances permitted or mandated by law). This school is in compliance with Title VI of the Civil Rights Act of 1964, which prohibits discrimination on the basis of race, color, or national origin; with the provisions of Title IX of the Educational Amendments of 1972, which prohibits discrimination on the basis of gender; with the provisions of Section 504 of the Rehabilitation Act of 1973, which prohibits discrimination on the basis of handicap; and with the American with Disabilities Act (ADA).

The following individuals have been designated to handle inquiries regarding the nondiscrimination policies:

American With Disabilities Act (ADA)/Section 504 - Equity- Title IX (Students) – Office of Civil Rights (OCR) Compliance Officer	**Title VI - Title IX (Employees) – Equal Employment Opportunity Commission (EEOC) Officer**
Helen Thomas, Special Needs Specialist Vidalia Campus 3001 East 1st Street, Vidalia Office 108 Phone: 912-538-3126 Email: Helen Thomas hthomas@southeasterntech.edu	Lanie Jonas, Director of Human Resources Vidalia Campus 3001 East 1st Street, Vidalia Office 138-B Phone: 912-538-3230 Email: Lanie Jonas ljonas@southeasterntech.edu

ACCESSIBILITY STATEMENT

Southeastern Technical College is committed to making course content accessible to individuals to comply with the requirements of Section 508 of the Rehabilitation Act of Americans with Disabilities Act (ADA). If you find a problem that prevents access, please contact the course instructor.

GRIEVANCE PROCEDURES

Grievance procedures can be found in the Catalog and Handbook located on Southeastern Technical College's website.

ACCESS TO TECHNOLOGY

Students can now access Blackboard, Remote Lab Access, Student Email, Library Databases (Galileo), and BannerWeb via the mySTC portal or by clicking the Current Students link on the Southeastern Technical College (STC) Website (www.southeasterntech.edu).

TECHNICAL COLLEGE SYSTEM OF GEORGIA (TCSG) GUARANTEE/WARRANTY STATEMENT

The Technical College System of Georgia guarantees employers that graduates of State Technical Colleges shall possess skills and knowledge as prescribed by State Curriculum Standards. Should any graduate employee within two years of graduation be deemed lacking in said skills, that student shall be retrained in any State Technical College at no charge for instructional costs to either the student or the employer.

GRADING POLICY

Assessment/Assignment	Percentage
Exams	35%
Laboratories	15%
Work Ethics	5%
Study Guides	10%
Final Exam*	35%

GRADING SCALE

Letter Grade	Range
A	90-100
B	80-89
C	70-79
D	60-69
F	0-59

DISCLAIMER STATEMENTS:

(1) Instructor reserves the right to change the syllabus and/or lesson plan as necessary.
(2) The official copy of the syllabus is located inside the student's online course shell or will be given to them during face to face class time the first day of the semester. The syllabus displayed in advance of the semester in a location other than the course you are enrolled in is for planning purposes only.

*** ELECTRONICS COMPETENCY EXAMS:**

The ELCR-1040 Final Exam is the **Electronics Systems Associate (ESA) Level 4 – Digital Circuits Exam**. The cost for taking this exam is **$35** payable to the STC Business Office before the last week of the semester. Please plan for this cost to complete the Digital Circuits course successfully. A grade of 75% or higher on this exam will result in the student being awarded their ESA Level 4 certificate from the International Society of Certified Electronics Technicians (ISCET).

A minimum grade of 70% is required for this exam. This exam will carry a 35% grading weight. Students who make a grade of <70 out of 100 points will be awarded a zero (0) for this exam and a failing grade for the class, which will require the student to retake ELCR 1040.

Students who wish to retake any ESA Exam in order to improve their grades to receive their Associate CET Certificate can do so at a cost of $15 per exam within two years of the original purchase of their test voucher for that exam.

Upon successful completion of all four parts of the ESA exams (i.e. ≥75% on ESA I through IV exams), the student is awarded their Associate CET Certificate from the ISCET.

ELCR-1040 Digital and Microprocessor Fundamentals
Spring Semester 2019 Lesson Plan

WEEK 1 (JAN IS JANUARY)

Date	Chapter / Lesson	Content	Assignments & Tests Due Dates	Competency Area
Jan 7	 **1.1** **1.2** **1.3** **1.4**	Class Introduction – Syllabi, Outline, Work Ethics, Rules, and Regulations Coverage Section 1.1 – Digital & Analog Quantities Section 1.2 – Binary Digits, Logic Levels, & Digital Waveforms Section 1.3 – Basic Logic Functions Section 1.4 – Combinational and Sequential Logic Functions	**[On BLACKBOARD]** Read / Review **Getting Started** POST to appropriate **Message Boards** **Read Sections 1.1 – 1.4**	1,4,5, b,c
Jan 8			**Read Sections 1.5 – 1.8**	
Jan 9	**1.5** **1.6** **1.7** **1.8**	Section 1.5 – Intro to Programmable Logic Section 1.6 – Fixed-Function Logic Devices Section 1.7 – Test and Measurement Instruments Section 1.8 – Introduction to Troubleshooting	**Do Chapter 1 Self Test** **Do Chapter 1 Study Guides**	1,4,5, b,c
Jan 10			**Study for Chapter 1 Test**	

WEEK 2

Date	Chapter / Lesson	Content	Assignments & Tests Due Dates	Competency Area
Jan 14	**1**	**Chapter 1 Test** **LabVolt (DLF) Intro to the Circuit Board**	**Take Chapter 1 Test**	1,4,5, a,b,c
Jan 15			**Read Sections 2.1 – 2.5**	
Jan 16	**2.1** **2.2** **2.3** **2.4** **2.5**	Section 2.1 – Decimal Numbers Section 2.2 – Binary Numbers Section 2.3 – Decimal-to-Binary Conversion Section 2.4 – Binary Arithmetic Section 2.5 – Complements of Binary Numbers		1,12, b,c
Jan 17			**Read Sections 2.1 – 2.5**	

WEEK 3

Date	Chapter / Lesson	Content	Assignments & Tests Due Dates	Competency Area
Jan 21	None	**Holiday – MLK Day**	**Holiday – MLK Day**	None
Jan 22			**Read Sections 2.6 – 2.9**	
Jan 23	**2.6** **2.7** **2.8** **2.9**	Section 2.6 – Signed Numbers Section 2.7 – Arithmetic Oper with Signed #s Section 2.8 – Hexadecimal Numbers Section 2.9 – Octal Numbers		1,12, b,c
Jan 24			**Read Sections 2.10 – 2.12**	
Jan 28	**2.10** **2.11** **2.12**	Section 2.10 – Binary Coded Decimal (BCD) Section 2.11 – Digital Codes Section 2.12 – Error Codes		1,12, b,c

WEEK 4 (FEB IS FEBRUARY)

Date	Chapter / Lesson	Content	Assignments & Tests Due Dates	Competency Area
Jan 29			**Do Chapter 2 Self Test** **Do Chapter 2 Study Guides** **Study for Chapter 2 Test**	
Jan 30	**2**	**Chapter 2 Test**	**Take Chapter 2 Test**	1,12, b,c
Jan 31			**Read Sections 3.1 – 3.5**	
Feb 4	**3.1** **3.2** **3.3** **3.4** **3.5**	Section 3.1 – The Inverter Section 3.2 – The AND Gate Section 3.3 – The OR Gate Section 3.4 – The NAND Gate Section 3.5 – The NOR Gate **LabVolt (DLF) Fundamental Logic Elements**		2,4,5, a,b,c

WEEK 5

Date	Chapter / Lesson	Content	Assignments & Tests Due Dates	Competency Area
Feb 5			**Read Sections 3.6 – 3.8**	
Feb 6	**3.6** **3.7** **3.8** **3.9**	Section 3.6 – The Exclusive-OR & Exclusive-NOR Gate Section 3.7 – Programmable Logic Section 3.8 – Fixed-Function Logic Gates Section 3.9 – Troubleshooting **LabVolt (DLF) Exclusive-OR / NOR Gates**		2,4,5, a,b,c
Feb 7			**Do Chapter 3 Self Test** **Do Chapter 3 Study Guides** **Study for Chapter 3 Test**	
Feb 11	**3**	**Chapter 3 Test**	**Take Chapter 3 Test**	2,4,5, b,c

WEEK 6

Date	Chapter / Lesson	Content	Assignments & Tests Due Dates	Competency Area
Feb 12			**Read Sections 4.1 – 4.6**	
Feb 13	**4.1** **4.2** **4.3** **4.4** **4.5** **4.6**	Section 4.1 – Boolean Operations & Expressions Section 4.2 – Laws & Rules of Boolean Algebra Section 4.3 – DeMorgan's Theorems Section 4.4 – Boolean Analysis of Logic Circuits Section 4.5 – Logic Simplification Using Boolean Algebra Section 4.6 – Standard Forms of Boolean Expressions		2,3, b,c
Feb 14			**Read Sections 4.7 – 4.12**	
Feb 18	**4.7** **4.8** **4.9** **4.10** **4.11** **4.12**	Section 4.7 – Boolean Expressions & Truth Tables Section 4.8 – The Karnaugh Map Section 4.9 – Karnaugh Map SOP Minimization Section 4.10 – Karnaugh Map POS Minimization Section 4.11 – The Quine-McCluskey Method Section 4.12 – Boolean Expressions with VHDL		2,3, b,c

WEEK 7

Date	Chapter / Lesson	Content	Assignments & Tests Due Dates	Competency Area
Feb 19			**Do Chapter 4 Self Test** **Do Chapter 4 Study Guides** **Study for Chapter 4 Test**	
Feb 20	**4**	**Chapter 4 Test**	**Take Chapter 4 Test**	2,3, b,c
Feb 21			**Read Sections 5.1 – 5.3**	
Feb 25	**5.1** **5.2** **5.3**	Section 5.1 – Basic Comb Logic Circuits Section 5.2 – Implementing Comb Logic Section 5.3 – The Universal Property of NAND and NOR Gates		2,3,5,12, b,c

WEEK 8 (MAR IS MARCH)

Date	Chapter / Lesson	Content	Assignments & Tests Due Dates	Competency Area
Feb 26			**Read Sections 5.4 – 5.7**	
Feb 27	**5.4** **5.5** **5.6** **5.7**	Section 5.4 – Combinational Logic using NAND and NOR Gates Section 5.5 – Pulse Waveform Operation Section 5.6 – Combinational Logic with VHDL Section 5.7 – Troubleshooting		2,3,5,12, b,c
Feb 28		**MID-TERM**	**Do Chapter 5 Self Test** **Do Chapter 5 Study Guides** **Study for Chapter 5 Test**	
Mar 4	**5**	**Chapter 5 Test**	**Take Chapter 5 Test**	2,3,5,12, b,c

WEEK 9

Date	Chapter / Lesson	Content	Assignments & Tests Due Dates	Competency Area
Mar 5			**Read Sections 6.1 – 6.4**	
Mar 6	**6.1** **6.2** **6.3** **6.4**	Section 6.1 – Half and Full Adders Section 6.2 – Parallel Binary Adders Section 6.3 – Ripple Carry and Look-Ahead Carry Adders Section 6.4 – Comparators **LabVolt (DCF1) 4-Bit Adder** **LabVolt (DCF1) 4-Bit Comparator**		2,5,8,9, a,b,c
Mar 7			**Read Sections 6.5 thru 6.7**	
Mar 11	**6.5** **6.6** **6.7**	Section 6.5 – Decoders Section 6.6 – Encoders Section 6.7 – Code Converters **LabVolt (DCF2) Decoder & Priority Encoder**		2,5,8,9, a,b,c

WEEK 10

Date	Chapter / Lesson	Content	Assignments & Tests Due Dates	Competency Area
Mar 12			**Read Sections 6.8 – 6.11**	
Mar 13	**6.8** **6.9** **6.10** **6.11**	Section 6.8 – Multiplexers (Data Selectors) Section 6.9 – Demultiplexers Section 6.10 – Parity Generators / Checkers Section 6.11 – Troubleshooting **LabVolt (DCF2) Multiplexer & Demultiplexer** **LabVolt (DCF2) Parity Generator / Checker**	**Do Chapter 6 Self Test** **Do Chapter 6 Study Guides** **Study for Chapter 6 Test**	2,5,8,9, a,b,c
Mar 14	**None**	STAFF DEVELOPMENT DAY (No Electronics Classes)	STAFF DEVELOPMENT DAY (No Electronics Classes)	None
Mar 18	**6**	**Chapter 6 Test**	**Take Chapter 6 Test**	2,5,8,9, b,c
Mar 19	**6**	**65% Drop Deadline for Classes**	**Read Sections 7.1 – 7.4**	5,6,12, a,b,c

WEEK 11

Date	Chapter / Lesson	Content	Assignments & Tests Due Dates	Competency Area
Mar 20	**7.1** **7.2** **7.3** **7.4**	Section 7.1 – Latches Section 7.2 – Flip-Flops Section 7.3 – Flip-Flop Operating Characteristics Section 7.4 – Flip-Flop Applications **LabVolt (DLF) Flip-Flops**		5,6,12, a,b,c
Mar 21			**Read Sections 7.5 – 7.7**	
Mar 25	**7.5** **7.6** **7.7**	Section 7.5 – One-Shots Section 7.6 – The Astable Multivibrator Section 7.7 – Troubleshooting **LabVolt (DLF) J-K Flip-Flop**		5,6,12, a,b,c
Mar 26			**Do Chapter 7 Self Test** **Do Chapter 7 Study Guides** **Study for Chapter 7 Test**	

WEEK 12 (APR IS APRIL)

Date	Chapter / Lesson	Content	Assignments & Tests Due Dates	Competency Area
Mar 27	**7**	**Chapter 7 Test** **WORK ETHICS - SESSION 1**	**Take Chapter 7 Test**	5,6,12 a,b,c
Mar 28			**Read Sections 8.1 – 8.4**	
Apr 1 – 4	None	**SPRING BREAK**	**SPRING BREAK**	None
Apr 8	**8.1** **8.2** **8.3** **8.4**	Section 8.1 – Shift Register Operations Section 8.2 – Types of Shift Register Data I/Os Section 8.3 – Bidirectional Shift Registers Section 8.4 – Shift Register Counters **LabVolt (DLF) 4-Bit Shift Register**		6,7, a,b,c
Apr 9			**Read Sections 8.5 – 8.7**	

WEEK 13

Date	Chapter / Lesson	Content	Assignments & Tests Due Dates	Competency Area
Apr 10	**8.5** **8.6** **8.7**	Section 8.5 – Shift Register Applications Section 8.6 – Shift Register Counters Section 8.7 – Troubleshooting		6,7, b,c
Apr 11			**Do Chapter 8 Self Test** **Do Chapter 8 Study Guides** **Study for Chapter 8 Test**	
Apr 15	**8**	**Chapter 8 Test**	**Take Chapter 8 Test**	6,7,9,10, b,c
Apr 16			**Read Sections 9.1 – 9.5**	

WEEK 14

Date	Chapter / Lesson	Content	Assignments & Tests Due Dates	Competency Area
Apr 17	**9.1** **9.2** **9.3** **9.4** **9.5**	Section 9.1 – Finite State Machines Section 9.2 – Asynchronous Counters Section 9.3 – Synchronous Counters Section 9.4 – Up/Down Synchronous Counters Section 9.5 – Design of Synchronous Counters **LabVolt – DLF – Asynchronous Ripple Counter**		6,7,9,10, a,b,c
Apr 18			**Read Sections 9.6 – 9.10**	
Apr 22	**9.6** **9.7** **9.8** **9.9** **9.10**	Section 9.6 – Cascaded Counters Section 9.7 – Counter Decoding Section 9.8 – Counter Applications Section 9.9 – Logic Symbols with Dep. Notation Section 9.10 – Troubleshooting **LabVolt – DLF – Synchronous Counter**	**Do Chapter 9 Self Test** **Do Chapter 9 Study Guides** **Study for Chapter 9 Test**	6,7,9,10, a,b,c
Apr 23				

WEEK 15

Date	Chapter / Lesson	Content	Assignments & Tests Due Dates	Competency Area
Apr 24	**9**	**Chapter 9 Test** **WORK ETHICS - SESSION 2 & Exam** ISCET ESA Exam Review	**Take Chapter 9 Test** **Read Sections 12.1 – 12.5**	6,7, b,c
Apr 25				
Apr 29	**12.1** **12.2** **12.3** **12.4** **12.5**	Section 12.1 – Analog-to-Digital Conversion Section 12.2 – Methods of A/D Conversion Section 12.3 – Methods of D/A Conversion Section 12.4 – Digital Signal Processing Section 12.5 – The Digital Signal Processor	**Do Chapter 12 Self Test** **Do Chapter 12 Study Guides** **Study for Chapter 12 Test**	11,12, b,c
Apr 30	**12**	**Chapter 12 Test** **Semester Classes End**	**Take Chapter 12 Test** **Study for Final Exam**	11,12, a,b,c

FINALS WEEK

Date	Chapter /Lesson	Content	Assignments & Tests Due Dates	Competency Area
May 1	**1 – 9, 12**	**Digital Circuits Final Exam [Proctored]** **ISCET ESA-4 Exam**	**9:00 AM Test Time**	1-12, b,c
May 2	**1 – 9, 12**	**Digital Circuits Final Exam [Proctored]** **ISCET ESA-4 Exam**	**1:00 PM Test Time**	1-12, b,c

COMPETENCY AREAS:

1. Binary Arithmetic
2. Logic Gates and Truth Tables
3. Boolean Algebra and Minimization Techniques
4. Logic Families
5. Digital Test Equipment
6. Flip-Flops
7. Counters
8. Multiplexers & De-multiplexers
9. Encoding & Decoding
10. Displays
11. Analog-to-Digital and Digital-to-Analog Conversions
12. Microprocessor Based Systems and Architecture

GENERAL CORE EDUCATIONAL COMPETENCIES:

a) The ability to utilize standard written English.
b) The ability to solve practical mathematical problems.
c) The ability to read, analyze, and interpret information.