ELCR 1040 – Digital and Microprocessor Fundamentals
COURSE SYLLABUS
SPRING SEMESTER 2016 (201614)

Semester:	**Spring 2016 / 201614**
Course Title:	**Digital and Microprocessor Fundamentals**
Course Number:	**ELCR 1040**
Credit Hr / Min:	**5 hr / 5250 min**
Class Location:	**RMTC Room 827**
Class Meets:	**MW, 5 to 7:55 p.m.**
CRN:	**40247**

Instructor:	**William Greene**
Office Hours:	**Mon –Thurs** 11:00 am – 12:00 pm
	Mon & Wed 1:00 pm – 3:00 pm
Office:	**RMTC Room 822, Vidalia Campus**
E-mail:	**wgreene@southeasterntech.edu**
Phone:	**912-538-3102 FAX: 912-538-3106**
	Preferred contact method is e-mail

REQUIRED TEXTS: *Digital Fundamentals, 11th ed.*
by Thomas L. Floyd, published by Prentice Hall,
ISBN# 0-13-273796-5

OPTIONAL SOFTWARES: National Instruments MultiSim Software Version 10, Student Suite (or higher)

REQUIRED SUPPLIES: Engineering / Scientific Calculator**, TI-83 Plus Graphing Calculator**. This calculator is required for the mathematics classes associated with the Electronics programs.

COURSE DESCRIPTION: This course is designed to provide sufficient coverage of digital electronics and microprocessor fundamentals. Digital fundamentals will introduce basic topics such as binary topics such as binary arithmetic, logic gates and truth tables, Boolean algebra and minimization techniques, logic families, and digital test equipment. Upon completion of the foundational digital requirements, a more advanced study of digital devices and circuits will include such topics as flip-flops, counters, multiplexers and de-multiplexers, encoding and decoding, displays, and analog to digital and digital to analog conversions. Students will also explore the basic architecture and hardware concepts of the microprocessor.

PREREQUISITES: ELCR-1020 **CO-REQUISITES**: ELCR-1030

MAJOR COURSE COMPETENCIES / COURSE OUTLINE:

1. Binary Arithmetic
2. Logic Gates & Truth Tables
3. Boolean Algebra & Minimization Techniques
4. Logic Families
5. Digital Test Equipment
6. Flip-Flops
7. Counters
8. Multiplexers & De-multiplexers
9. Encoding & Decoding
10. Displays
11. Analog-to-Digital and Digital-to-Analog Conversions
12. Microprocessor Based Systems and Architecture

GENERAL EDUCATION CORE COMPETENCIES: STC has identified the following general education core competencies that graduates will attain:

1. The ability to utilize standard written English.
2. The ability to solve practical mathematical problems.
3. The ability to read, analyze, and interpret information.

STUDENT REQUIREMENTS: Students are expected to complete all tests and comprehensive problems by the due dates. A ten point penalty will be assessed for each day a comprehensive problem is late. There are no makeup tests. **Tests are made available for several days; therefore, there are no**

makeup tests. Students who miss a test will be assigned a grade of zero. Students are responsible for policies and procedures included in the *STC E-Catalog*. **All students must** pledge that they have read and understand the *STC Online Orientation* within the first five days of class. **All students are responsible for checking e-mails and Blackboard announcements DAILY.**

WORK ETHICS: The Technical College System of Georgia instructs and evaluates students on work ethics in all programs of study. Ten work ethics traits have been identified and defined as essential for student success: appearance, attendance, attitude, character, communication, cooperation, organizational skills, productivity, respect, and teamwork. Students will be required to take a work ethics exam as marked in the lesson plan. A grade of 70 or better is required to complete the work ethics requirements for this class.

ATTENDANCE GUIDELINES: Class attendance is a very important aspect of a student's success. Being absent from class prevents students from receiving the full benefit of a course and also interrupts the learning process. Southeastern Technical College considers both tardiness and leaving early as types of absenteeism. Responsibility for class attendance rests with the student. Regular and punctual attendance at all scheduled classes is required for student success. Students will be expected to complete all work required by the instructor as described in the individual course syllabus.

Instructors have the right to give unannounced quizzes/assignments. Students who miss an unannounced quiz or assignment will receive a grade of 0. Students who stop attending class, but do not formally withdraw, may receive a grade of F and face financial aid repercussions in upcoming semesters.

Instructors are responsible for determining whether missed work may be made up and the content and dates for makeup work is at the discretion of the instructor.

Students will not be withdrawn by an instructor for attendance; however, all instructors will keep records of graded assignments and student participation in course activities. The completion dates of these activities will be used to determine a student's last date of attendance in the event a student withdraws, stops attending, or receives an F in a course.

SPECIFIC ABSENCES: Provisions for Instructional Time missed because of documented absences due to jury duty, military duty, court duty, or required job training will be made at the discretion of the instructor.

SPECIAL NEEDS: *Students with disabilities who believe that they may need accommodations in this class based on the impact of a disability are encouraged to contact Helen Thomas, Room 108 Vidalia Campus, 912-538-3126, or Jan Brantley, Room 1208 Swainsboro Campus, 478-289-2274, to coordinate reasonable accommodations.*

PREGNANCY: Southeastern Technical College does not discriminate on the basis of pregnancy. However, we can offer accommodations to students who are pregnant that need special consideration to successfully complete the course. If you think you will need accommodations due to pregnancy, please advise me and make appropriate arrangements with the Special Needs Office. Swainsboro Campus: Jan Brantley, Room 1208, (478) 289-2274 -- Vidalia Campus: Helen Thomas, Room 108, (912) 538-3126.

WITHDRAWAL PROCEDURE: Students wishing to officially withdraw from a course(s) or all courses after the drop/add period and prior to the 65% portion of the semester (date will be posted on the school calendar) must speak with a Career Counselor in Student Affairs and complete a Student Withdrawal Form. A grade of "W" is assigned when the student completes the withdrawal form from the course.

Students who are dropped from courses due to attendance (see your course syllabus for attendance policy) after drop/add until the 65% point of the semester will receive a "W" for the course. Abandoning a course(s) instead of following official withdrawal procedures may result in a grade of 'F' being assigned.

After the 65% portion of the semester, the student will receive a grade for the course. (Please note: A zero will be given for all missed assignments.)

There is no refund for partial reduction of hours. Withdrawals may affect students' eligibility for financial aid for the current semester and in the future, so a student must also speak with a representative of the

Financial Aid Office to determine any financial penalties that may be accessed due to the withdrawal. All grades, including grades of 'W', will count in attempted hour calculations for the purpose of Financial Aid.

Remember - Informing your instructor that you will not return to his/her course does not satisfy the approved withdrawal procedure outlined above.

MAKEUP GUIDELINES (Tests, quizzes, homework, projects, etc…): Students are required to take all tests and complete all assignments scheduled during the semester. Failure to take Tests/Exam(s) and complete assignments **will result in a grade of zero. There will be no makeup of assignments or EXAMS.** If Internet or browser failure occurs, contact instructor immediately. A decision will be made at that time if the exam will be reset. Instructor reserves the right to deduct points from the exam scores for exceeding the scheduled time limit on the exam and/or requiring student to come to campus to take the final exam. Note: If student notifies instructor about exam problems because of technical issues after the due date or on the last day of the semester, the student will **NOT** be allowed to make-up the exam. **No exceptions! Assignments must be turned in on the assigned date and will not be accepted late, a grade of zero will be given. ALL Assignments are due according to the lesson plan.**

ACADEMIC DISHONESTY POLICY: The STC Academic Dishonesty Policy states *All forms of academic dishonesty, including but not limited to cheating on tests, plagiarism, collusion, and falsification of information, will call for discipline.* The policy can also be found in the *STC Catalog and Student Handbook.*

Procedure for Academic Misconduct
The procedure for dealing with academic misconduct and dishonesty is as follows:

--First Offense—
Student will be assigned a grade of "0" for the test or assignment. Instructor keeps a record in course/program files and notes as first offense. The instructor will notify the student's program advisor, academic dean, and the Registrar at the student's home campus. The Registrar will input the incident into Banner for tracking purposes.

--Second Offense—
Student is given a grade of "WF" for the course in which offense occurs. The instructor will notify the student's program advisor, academic dean, and the Registrar at the student's home campus indicating a "WF" has been issued as a result of second offense. The Registrar will input the incident into Banner for tracking purposes.

--Third Offense—
Student is given a grade of "WF" for the course in which the offense occurs. The instructor will notify the student's program advisor, academic dean, and the Registrar at the student's home campus indicating a "WF" has been issued as a result of second offense. The Vice President for Student Affairs, or designee, will notify the student of suspension from college for a specified period of time. The Registrar will input the incident into Banner for tracking purposes.

STATEMENT OF NON-DISCRIMINATION
Southeastern Technical College does not discriminate on the basis of race, color, creed, national or ethnic origin, gender, religion, disability, age, disabled veteran, veteran of Vietnam Era or citizenship status, (except in those special circumstances permitted or mandated by law). This school is in compliance with Title VI of the Civil Rights Act of 1964, which prohibits discrimination on the basis of race, color, or national origin; with the provisions of Title IX of the Educational Amendments of 1972, which prohibits discrimination on the basis of gender; with the provisions of Section 504 of the Rehabilitation Act of 1973, which prohibits discrimination on the basis of handicap; and with the American with Disabilities Act (ADA).

GRIEVANCE PROCEDURES: Grievance procedures can be found in the Catalog and Handbook located on STC's website.

ACCESS TO TECHNOLOGY: Students can now access Blackboard, Remote Lab Access, Student Email, Library Databases (Galileo), and BannerWeb via the mySTC portal or by clicking the Current Students link on the STC website at www.southeasterntech.edu.

TCSG GUARANTEE/WARRANTY STATEMENT:
The Technical College System of Georgia guarantees employers that graduates of State Technical Colleges shall possess skills and knowledge as prescribed by State Curriculum Standards. Should any graduate employee within two years of graduation be deemed lacking in said skills, that student shall be retrained in any State Technical College at no charge for instructional costs to either the student or the employer.

ELCR 1040 GRADING POLICY:

Exams	**35%**
Labs	**15%**
Work Ethics	**5%**
Study Guides	**10%**
Final Exam	**35% ***
	100%

GRADING SCALE:

A (90-100)
B (80-89)
C (70-79)
D (60-69)
F (0-59)

For **any** course to count as credit for graduation, student must make a C or higher in the course.

*** PROGRAM CAPSTONE EXAM Grade of 70 or Higher REQUIRED or you must repeat the course.**

ELECTRONICS COMPETENCY EXAMS:

*** The ELCR 1040 Final Exam (for Digital II) is the ESA Part IV – Digital Exam. The cost for taking this exam is $35 payable to the STC Business Office before the last week of the quarter. Please plan for this cost to complete the Digital Electronics series of classes successfully. A grade of 75% or higher on this exam will result in the student being awarded their ESA IV certificate from the ISCET.**

A minimum grade of 70% is required for this exam. This exam will carry a 35% grading weight. Students who make a grade of <70 out of 100 points will be awarded a zero (0) for this exam and a failing grade for the class, which will require the student to retake ELCR 1040.

Upon successful completion of all four parts of the ESA exams (i.e. ≥75% on ESA I through IV exams), the student is awarded their Associate CET Certificate from the ISCET.

Students who wish to retake any ESA Exam in order to improve their grades to receive their Associate CET Certificate can do so at a cost of $15 per exam within one year of the original purchase of their test voucher for that exam.

Disclaimer Statements

(1) Instructor reserves the right to change the syllabus and/or lesson plan as necessary.
(2) The official copy of the syllabus is located inside the student's online course shell or will be given to them during face to face class time the first day of the semester. The syllabus displayed in advance of the semester in a location other than the course you are enrolled in is for planning purposes only.

ELCR-1040 – Digital and Microprocessor Fundamentals LESSON PLAN Spring Semester 2016 (CRN 40247)				
Color Codes: **Black = Assignments & Information,** **Blue = Graded Assignments**				
Date	Chapter / Lesson	**Content**	**Assignments & Tests (Due Dates)**	*Comp. Area
WEEK 1				
Jan 11	**1.1** **1.2** **1.3** **1.4**	**Class Introduction – Syllabi, Outline, Work Ethics, Rules, and Regulations Coverage** **Section 1.1 – Digital & Analog Quantities** **Section 1.2 – Binary Digits, Logic Levels, & Digital Waveforms** **Section 1.3 – Basic Logic Functions** **Section 1.4 – Combinational and Sequential Logic Functions**	**[On Blackboard]** Read / Review **Announcements** POST to appropriate **Message Boards** **Read Sections 1.1 thru 1.4**	1,4,5, b,c
12			**Read Sections 1.5 thru 1.8**	
13	**1.5** **1.6** **1.7** **1.8**	**Section 1.5 – Intro to Programmable Logic** **Section 1.6 – Fixed-Function Logic Devices** **Section 1.7 – Test and Measurement Instruments** **Section 1.8 – Introduction to Troubleshooting**	**Do Chapter 1 Self Test** **Do Chapter 1 Study Guides**	1,4,5, b,c
14			**Study for Chapter 1 Test**	
WEEK 2				
Jan 18		**HOLIDAY**		
19			**Study for Chapter 1 Test**	
20	**1**	**Chapter 1 Test** **LabVolt – DLF – Introduction to the Circuit Board**	**Take Chapter 1 Test**	1,4,5, a,b,c
21			**Read Sections 2.1 thru 2.5**	
25	**2.1** **2.2** **2.3** **2.4** **2.5**	**Section 2.1 – Decimal Numbers** **Section 2.2 – Binary Numbers** **Section 2.3 – Decimal-to-Binary Conversion** **Section 2.4 – Binary Arithmetic** **Section 2.5 – Complements of Binary Numbers**	**ALL Chapter 1 Assignments DUE**	1,12, b,c
WEEK 3				
Jan 26			**Read Sections 2.6 thru 2.9**	
27	**2.6** **2.7** **2.8** **2.9**	**Section 2.6 – Signed Numbers** **Section 2.7 – Arithmetic Oper with Signed #s** **Section 2.8 – Hexadecimal Numbers** **Section 2.9 – Octal Numbers**		1,12, b,c
28			**Read Sections 2.10 – 2.12**	
Feb 1	**2.10** **2.11** **2.12**	**Section 2.10 – Binary Coded Decimal (BCD)** **Section 2.11 – Digital Codes** **Section 2.12 – Error Codes**		1,12, b,c

WEEK 4				
Feb 2			**Do Chapter 2 Self Test** **Do Chapter 2 Study Guides** **Study for Chapter 2 Test**	
3	**2**	**Chapter 2 Test**	**Take Chapter 2 Test**	1,12, b,c
4			**Read Sections 3.1 thru 3.5** **ALL Chapter 2 Assignments DUE**	
8	**3.1** **3.2** **3.3** **3.4** **3.5**	**Section 3.1 – The Inverter** **Section 3.2 – The AND Gate** **Section 3.3 – The OR Gate** **Section 3.4 – The NAND Gate** **Section 3.5 – The NOR Gate** **LabVolt – DLF – Fundamental Logic Elements**		2,4,5, a,b,c
WEEK 5				
Feb 9			**Read Sections 3.6 thru 3.8**	
10	**3.6** **3.7** **3.8** **3.9**	**Section 3.6 – The Exclusive-OR & Exclusive-NOR Gate** **Section 3.7 – Programmable Logic** **Section 3.8 – Fixed-Function Logic Gates** **Section 3.9 – Troubleshooting** **LabVolt – DLF – Exclusive-OR / NOR Gates**		2,4,5, a,b,c
11			**Do Chapter 3 Self Test** **Do Chapter 3 Study Guides** **Study for Chapter 3 Test**	
15	**3**	**Chapter 3 Test**	**Take Chapter 3 Test**	2,4,5, b,c
WEEK 6				
Feb 16			**Read Sections 4.1 thru 4.6** **ALL Chapter 3 Assignments DUE**	
17	**4.1** **4.2** **4.3** **4.4** **4.5** **4.6**	**Section 4.1 – Boolean Operations & Expressions** **Section 4.2 – Laws & Rules of Boolean Algebra** **Section 4.3 – DeMorgan's Theorems** **Section 4.4 – Boolean Analysis of Logic Circuits** **Section 4.5 – Logic Simplification Using Boolean Algebra** **Section 4.6 – Standard Forms of Boolean Expressions**		2,3, b,c
18			**Read Sections 4.7 thru 4.12**	
22	**4.7** **4.8** **4.9** **4.10** **4.11** **4.12**	**Section 4.7 – Boolean Expressions & Truth Tables** **Section 4.8 – The Karnaugh Map** **Section 4.9 – Karnaugh Map SOP Minimization** **Section 4.10 – Karnaugh Map POS Minimization** **Section 4.11 – The Quine-McCluskey Method** **Section 4.12 – Boolean Expressions with VHDL**		2,3, b,c

WEEK 7				
Feb 23			**Do Chapter 4 Self Test** **Do Chapter 4 Study Guides** **Study for Chapter 4 Test**	
24	**4**	**Chapter 4 Test**	**Take Chapter 4 Test**	2,3, b,c
25			**Read Sections 5.1 thru 5.3** **ALL Chapter 4 Assignments DUE**	
29	**5.1** **5.2** **5.3**	**Section 5.1 – Basic Comb Logic Circuits** **Section 5.2 – Implementing Comb Logic** **Section 5.3 – The Universal Property of NAND and NOR Gates**		2,3,5,12, b,c
WEEK 8				
Mar 1			**Read Sections 5.4 thru 5.7**	
2	**5.4** **5.5** **5.6** **5.7**	**Section 5.4 – Combinational Logic using NAND and NOR Gates** **Section 5.5 – Pulse Waveform Operation** **Section 5.6 – Combinational Logic with VHDL** **Section 5.7 – Troubleshooting**		2,3,5,12, b,c
3		**MID-TERM**	**Do Chapter 5 Self Test** **Do Chapter 5 Study Guides** **Study for Chapter 5 Test**	
7	**5**	**Chapter 5 Test**	**Take Chapter 5 Test**	2,3,5,12, b,c
WEEK 9				
Mar 8			**Read Sections 6.1thru 6.4** **ALL Chapter 5 Assignments DUE**	
9	**6.1** **6.2** **6.3** **6.4**	**Section 6.1 – Half and Full Adders** **Section 6.2 – Parallel Binary Adders** **Section 6.3 – Ripple Carry and Look-Ahead Carry Adders** **Section 6.4 – Comparators** **LabVolt – DCF1 – 4-Bit Adder** **LabVolt – DCF1 – 4-Bit Comparator**		2,5,8,9, a,b,c
10			**Read Sections 6.5 thru 6.7**	
14	**6.5** **6.6** **6.7**	**Section 6.5 – Decoders** **Section 6.6 – Encoders** **Section 6.7 – Code Converters** **LabVolt – DCF2 – Decoder & Priority Encoder**		2,5,8,9, a,b,c
WEEK 10				
Mar 15			**Read Sections 6.8 thru 6.11**	
16	**6.8** **6.9** **6.10** **6.11**	**Section 6.8 – Multiplexers (Data Selectors)** **Section 6.9 – Demultiplexers** **Section 6.10 – Parity Generators / Checkers** **Section 6.11 – Troubleshooting** **LabVolt – DCF2 – Multiplexer & Demultiplexer** **LabVolt – DCF2 – Parity Generator / Checker**		2,5,8,9, a,b,c

Mar 17			**Do Chapter 6 Self Test** **Do Chapter 6 Study Guides** **Study for Chapter 6 Test**	
21	**6**	**Chapter 6 Test** **65% Drop Deadline for Classes**	**Take Chapter 6 Test**	2,5,8,9, b,c
		WEEK 11		
Mar 22			**Read Sections 7.1 thru 7.4** **ALL Chapter 6 Assignments DUE**	
23	**7.1** **7.2** **7.3** **7.4**	**Section 7.1 – Latches** **Section 7.2 – Flip-Flops** **Section 7.3 – Flip-Flop Operating Characteristics** **Section 7.4 – Flip-Flop Applications** **LabVolt – DLF – Flip-Flops**		5,6,12, a,b,c
24			**Read Sections 7.5 thru 7.7**	
28		**SPRING BREAK – NO CLASSES**		
29		**SPRING BREAK – NO CLASSES**		
30		**SPRING BREAK – NO CLASSES**		
31		**SPRING BREAK – NO CLASSES**		
Apr 4	**7.5** **7.6** **7.7**	**Section 7.5 – One-Shots** **Section 7.6 – The Astable Multivibrator** **Section 7.7 – Troubleshooting** **LabVolt – DLF – J-K Flip-Flop**		5,6,12, a,b,c
		WEEK 12		
Apr 5			**Do Chapter 7 Self Test** **Do Chapter 7 Study Guides** **Study for Chapter 7 Test**	
6	**7**	**Chapter 7 Test** **WORK ETHICS - SESSION 1**	**Take Chapter 7 Test**	5,6,12, a,b,c
7			**Read Sections 8.1thru 8.4** **ALL Chapter 7 Assignments DUE**	
11	**8.1** **8.2** **8.3** **8.4**	**Section 8.1 – Shift Register Operations** **Section 8.2 – Types of Shift Register Data I/Os** **Section 8.3 – Bidirectional Shift Registers** **Section 8.4 – Shift Register Counters** **LabVolt – DLF – 4-Bit Shift Register**		6,7, a,b,c
		WEEK 13		
Apr 12			**Read Sections 8.5 thru 8.7**	
13	**8.5** **8.6** **8.7**	**Section 8.5 – Shift Register Applications** **Section 8.6 – Shift Register Counters** **Section 8.7 – Troubleshooting**		6,7, b,c
14		**SPRING ACTIVITY DAY**	**Do Chapter 8 Self Test** **Do Chapter 8 Study Guides** **Study for Chapter 8 Test**	
18	**8**	**Chapter 8 Test**	**Take Chapter 8 Test**	6,7,9,10, b,c

WEEK 14				
Apr 19			**Read Sections 9.1 thru 9.5** **ALL Chapter 8 Assignments DUE**	
20	**9.1** **9.2** **9.3** **9.4** **9.5**	**Section 9.1 – Finite State Machines** **Section 9.2 – Asynchronous Counters** **Section 9.3 – Synchronous Counters** **Section 9.4 – Up/Down Synchronous Counters** **Section 9.5 – Design of Synchronous Counters** **LabVolt – DLF – Asynchronous Ripple Counter**		6,7,9,10, a,b,c
21			**Read Sections 9.6 thru 9.10**	
25	**9.6** **9.7** **9.8** **9.9** **9.10**	**Section 9.6 – Cascaded Counters** **Section 9.7 – Counter Decoding** **Section 9.8 – Counter Applications** **Section 9.9 – Logic Symbols with Dep. Notation** **Section 9.10 – Troubleshooting** **LabVolt – DLF – Synchronous Counter**	**Do Chapter 9 Self Test** **Do Chapter 9 Study Guides** **Study for Chapter 9 Test**	6,7,9,10, a,b,c
WEEK 15				
Apr 26	**9**	**Chapter 9 Test**	**Take Chapter 9 Test** **(Over this Weekend)** **Read Sections 12.1 thru 12.5**	6,7, b,c
27	**12.1** **12.2** **12.3** **12.4** **12.5**	**Section 12.1 – Analog-to-Digital Conversion** **Section 12.2 – Methods of A/D Conversion** **Section 12.3 – Methods of D/A Conversion** **Section 12.4 – Digital Signal Processing** **Section 12.5 – The Digital Signal Processor (DSP)**	**Do Chapter 12 Self Test** **Do Chapter 12 Study Guides** **Study for Chapter 12 Test**	11,12, b,c
28			**ALL Chapter 9 Assignments DUE**	
May 2	**12**	**Chapter 12 Test** **WORK ETHICS - SESSION 2 & Exam** **Semester Classes End**	**Take Chapter 12 Test** **Study for Final Exam** **ALL Chap 12 Assignments DUE**	11,12, a,b,c
FINALS WEEK				
May 4		**Digital Final Exam [Proctored]** **ESA – Level 4**	**9:00 AM to 12:00 PM** **Room 803 – Gillis Building**	1 – 12, b,c
May 5		**Digital Final Exam [Proctored]** **ESA – Level 4**	**2:00 PM to 5:00 PM** **Room 803 – Gillis Building**	1 – 12, b,c

*** Competency Areas:**

Electronics Technology Competency Areas:

1. Binary Arithmetic
2. Logic Gates and Truth Tables
3. Boolean Algebra and Minimization Techniques
4. Logic Families
5. Digital Test Equipment
6. Flip-Flops
7. Counters
8. Multiplexers & De-multiplexers
9. Encoding & Decoding
10. Displays
11. Analog-to-Digital and Digital-to-Analog Conversions
12. Microprocessor Based Systems and Architecture

General Core Competency Areas:

a. The ability to utilize standard written English.
b. The ability to solve practical mathematical problems.
c. The ability to read, analyze, and interpret information.